A DECODER FOR TRELLIS-BASED CHANNEL ENCODING

Abstract of the Disclosure

A system and method for decoding a channel bit stream efficiently performs trellis-based operations. The system includes a butterfly coprocessor and a digital signal processor. For trellis-based encoders, the system decodes a channel bit stream by performing operations in parallel in the butterfly coprocessor, at the direction of the digital signal processor. The operations are used in implementing the MAP algorithm, the Viterbi algorithm, and other soft- or hard-output decoding algorithms. The DSP may perform memory management and algorithmic scheduling on behalf of the butterfly coprocessor. The butterfly coprocessor may perform parallel butterfly operations for increased throughput. The system maintains flexibility, for use in a number of possible decoding environments.